WHAT IS CLAIMED IS:

1. An apparatus having a CPU and a bridge controller wherein the improvement comprises:

a clock generator generating a first clock signal for the CPU operating in one of AC power mode or battery power mode, and a second clock signal for the bridge controller, operating in one of AC power mode or battery power mode, wherein first and second clock signals are two distinct clock signals outputted by the clock generator and have different frequencies.

2. The apparatus of claim 1, wherein the bridge controller controls a clock speed of a bus for data communication among a plurality of peripheral devices of the portable device.

3. The apparatus of claim 1, wherein the improvement further comprises a first phase locked loop (PLL) receiving the first clock signal for the CPU and adjusting the first clock signal based on one of AC power mode and battery power mode.

4. The apparatus of claim 1, wherein the improvement further comprises a second phase locked loop (PLL) receiving the second clock signal for the bridge controller

and adjusting the second clock signal based on one of AC power mode and battery power mode.

5. The apparatus of claim 1, wherein the portable device further includes a video processor and the clock generator generates a third clock signal for the video processor, the third clock signal being distinct from the first and second clock signals and having a different frequency than the first and second clock signals.

6. The apparatus of claim 5, wherein the improvement further comprises a third phase locked loop (PLL) receiving the third clock signal and adjusting the third clock signal based on one of AC power mode and battery power mode.

7. The apparatus of claim 5, wherein the first clock signal has a higher frequency than the second clock signal and the second clock signal has a higher frequency than the third clock signal.

8. The apparatus of claim 4, wherein the second PLL increases the frequency of the second clock signal in the AC power mode or outputs the second clock signal without frequency adjustment in the battery power mode.

9. The apparatus of claim 4, wherein the second PLL decreases the frequency of the second clock signal in a battery power mode or outputs the second clock signal without frequency adjustment in the AC power mode.

10. The apparatus of claim 6, wherein the third PLL increases the frequency of the second clock signal in the AC power mode or outputs the third clock signal without frequency adjustment in the battery power mode.

11. The apparatus of claim 6, wherein the third PLL decreases the frequency of the second clock signal in a battery power mode or outputs the third clock signal without frequency adjustment in the AC power mode.

12. An apparatus having a CPU and a bridge controller, wherein the improvement comprises:

a clock generator generating a first clock signal; and

a clock adjustor receiving the first clock signal and operating in one of AC power mode or battery power mode, said clock adjustor generating a second clock signal for the CPU and a third clock signal for the bridge controller, wherein the second and third clock signals are two distinct clock signals outputted by the clock adjustor and have different frequencies.

13. The apparatus of claim 12, wherein the bridge controller controls a clock speed of a bus for data communication among a plurality of peripheral devices of the portable device.

14. The apparatus of claim 12, wherein the clock adjustor is a first phase locked loop (PLL).

15. The apparatus of claim 12, wherein the improvement further comprises a second phase locked loop (PLL) receiving the second clock signal for the CPU and adjusting the second clock signal based on one of AC power mode and battery power mode.

16. The apparatus of claim 12, wherein the portable device further includes a video processor and the clock adjustor generates a fourth clock signal for the video processor, the fourth clock signal being distinct from the second and third clock signals and having a different frequency than the second and third clock signals.

17. The apparatus of claim 16, wherein the second clock signal has a higher frequency than the third clock signal and the third clock signal has a higher frequency than the fourth clock signal.

18. The apparatus of claim 16, wherein the first and fourth clock signals have the same frequency.

19. A method for optimizing clock speed generation, comprising:

receiving a base clock signal;

multiplying the base clock signal by a first factor to produce a first higher frequency clock signal, wherein the first higher frequency clock signal is phase-locked with the base clock signal;

receiving a power mode signal indicating either an AC or a battery source; and

selectively outputting the first higher frequency clock signal to a first device when the AC source is indicated and outputting the base clock signal to the first device when the battery source is indicated.